

USING EDA THROUGHOUT PRODUCT LIFE-CYCLES

A High Level Overview

November, 2008

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The analysis software and design files successfully used in electronic design practice and cycles can also serve well during the rest of the product lifecycle (PLC). Programmatic elements to consider are introduced.

Essentially all modern circuitry in use today has been designed using the capabilities of electronic design automation (EDA) tools to meet the intended requirements. Generations of EDA tools have followed each other into engineering departments of every serious firm, and an entire industry has developed to supply these tools and support their use by these firms. Virtually every EE student in the last two decades and well before has been introduced to these tools in school, and there is general familiarity with their usage paradigm.

As their capabilities have evolved, the thrust of the EDA firms has been toward higher performance, more functionality, and more cost. "Strategic engagement" business models involving million-dollar-levels of annual contract fees allow EDA firms to deliver very deep involvement in design houses' engineering efforts. This pattern results in effective performance, and a cadre of highly specialized and skilled professionals who are the houses' de facto gurus for the circuits they design and move into production.

However, because the EDA software is so pricey and the engagements are so complicated, firms restrict the usage of the tools within the design functions, and other organizations that are active in the product life cycle, either in parallel or later in the cycle, often have little or no access to the files that represent the designs that have been generated. An obvious example rarely seen is the use of design files for stress analyses and FMEAs by reliability engineers. Comprehensive test failure resolution in high-criticality situations, such as TAAF projects, detailed assessment of pattern failure recurrences, and sneak-circuit incidents all can benefit from the ability of an adept analyst to "tweak" a full model of a circuit instead of relying on visually-accessed schematics, and pen-and-paper analyses. EMI properties can be more readily assessed by directly accessing circuit models, as can power dissipation and dynamic signal conditions. For military use in severely degraded, totally out-of-spec scenarios, model manipulation access, using a broadened-EDA-access approach, is a vast improvement over purely paper analyses.

What these all have in common is that they are in-hindsight-obvious additional ways to effectively make use of the existing design files when a worthwhile reason arises. These are expansions that bring more of a firm's (or agency's) professional talent into contact with the design modeling and performance characterization. It allows more detailed use of existing design files, involves more sets of eyes, and lowers the firm's dependence on the original designer, freeing her/him from sustaining burdens on completed designs. Thus, analysis software and design files can also serve well during the rest of the product lifecycle (PLC).

Where does the value lie in such activities? Several classes of challenges routinely arise in ongoing programs in military, aerospace, telecommunication, and medical areas. Unlike commercial consumer products, which quickly come and go, the aforementioned programs have significant NRE content, and long-term life usage needs to recover the costs invested. Military and medical programs have severe impact on users when they don't quite work as intended, so they also carry significant product qualification investments as part of the NRE. So, PLC use of design files is an improved way to address issues in parts obsolescence, pattern failure emergencies, retro-qualification of COTS products, and ex-post-facto agency requirements on subsequent or follow-on orders.

It is helpful to contemplate the absence of PLC use of EDA files in light of what actually happens. Production programs are routinely "surprised" by unbudgeted incidents, as above, that demand prompt addressing, at which time it is found that there is no technical expertise available, the documentation level is charitably described as "partial", obscure critical parameters lurk, the design has "evolved" over revisions, tolerance windows have meandered or shifted, and program-specific waivers or deviations abound. The signature blocks on the originally qualified versions have names unfamiliar to the current staff. Promotions, transfers, layoffs, H1-B departures and other items best left to HR all contribute. Organizational politics and lack of technical ownership do exist in real organizations. This sets the stage on which a firm's "technical firefighters" arrive to take action.

The whole point here is that the "technical portfolio" associated with any designed product can be systematized and raised to a higher level of effectiveness by focusing on the design files. Optimally, this can be done as a policy initiative enacted at program starts, but in reality it has to and will be done in most firms by grafting the approach opportunistically as a "pay-once-learning" response to issues that assert their seriousness by drawing senior management attention. This gives it an organic flavor, and suggests that the same intent in different firms will have quite different instantiations, which reflect the firms' working cultures. There may be an ideal core, which brings an agile responsiveness to a firm's operational needs without creating a bureaucratic layer of baggage that absorbs precious resources and distracts technical and managerial attention from their primary focus.

Details of a few representative program forms that can be implemented follow.

Focusing on SPICE (Simulation Program with Integrated Circuit Emphasis):

- Virtually every circuit in use was designed using EDA (Electronic Design Automation), and the core of EDA is the circuit analysis software.
- Associated design files are commonly preserved; if not, they can be generated from schematics, and validated against specs
- For many parts, vendors are providing SPICE parameters
- Many existing designs are ports of IC vendor app-note subcircuits, with passive part values directly copied in
- Most IC vendors now provide entire SPICE-modeled representative applications of their parts
- Use of ANY EDA modeling (not just the original EDA tool version) can bring improvement over "visual-scan" reviews of part-change impact

STRAIGHTFORWARD RECIPE

For virtually every EDA package in design use, there are compatible versions to support PLC uses (quite often the same EDA vendor will have an offering, or a license modification)

Recommended flow for addressing "incidents", or scoping out a program, is:

- Identify new questions, proposed change(s), or issues
- Determine scope of reviews and analyses to be revised
- Generate or acquire/resurrect suitable EDA model
- Characterize before/after by several simulation runs to elucidate significant features, or bring them out if the documentation package is "inadequate"
- Act on data, iterate as indicated

Life can be easier if you can stage a rehearsal to wring out your in-house issues

SPICE-SPECIFIC ENTRY-EXPLORATORY APPROACH

- Linear Technology offers SwCAD III for download FREE. Play with it – the price is right!
- PSPICE, MULTISIM (NI/ADI), TINA (TI), AIMSPICE, 5SPICE and many other firms provide node- or component-limited "student" versions, or time-constrained evaluations.
- The best choice is the one that most closely matches your design engineering group's development package. (Or, see if you can get an extra seat with them).
- Unless EXTENSIVE changes are involved, any SPICE flavor will do fine. Simulating changes is the point.
- The key is ability to modify parts on an interactive schematic, or to edit circuit-descriptive netlists.

SOME CASES THAT ARISE

EDA-accessible circuit/system dynamics to consider:

- Impact of capacitor ESR changes in switching regulators
- Changes in transient response, circuit stability, or EMI issues
- Compromises in performance windows, derating or EOL margins
- Possible changes in FMEA propagation
- Power dissipation reduction for "green" reasons
- ...more...dependent on specifics of case under study

One attractive feature that a comprehensive PLC-EDA program offers is the ability to keep the design engineers engaged through a full lifecycle of a product, which can be invaluable for developing the breadth of awareness of a business operation's many facets as training for the next generations of middle and senior managers. It makes design engineers, or any of the engineers connected along the cycle, able to move more broadly among the functional activities, and exposes them earlier in their careers to more elements of the spectrum of challenges the firm faces in its operations. This can be effective both in retention of valuable talent, and attracting a higher caliber of experienced talent that can appreciate its benefits and see its value to their career advancement.

KEY TAKEAWAY

The same analysis software so successfully established in electronic design practice can also serve well during the rest of the product lifecycle. No barriers exist except the choice to begin. And for helping you with this process, please call on the reliability consultants at Ops A La Carte to help.

BIOGRAPHIES

Bryan Stallard is a senior reliability consultant at Ops A La Carte with over 30 years experience in analysis, design, and testing of electronic products, spanning the scale from junction diodes to satellite bus systems. He has worked on aviation electronics displays (A-6, A-10, F16, F18, Cobra), radar-warning receivers (ALR-45, ALR-67, ALR74), and satellite families (INTELSAT, GOES, SUPERBIRD, Space Station) as circuit analyst, program reliability engineer, RF designer, component engineer, failure-lab analyst, and combination-activity roles. He is culturally familiar with military, NASA, commercial aerospace, semiconductor, and telecom practices and expectations. Employers included Kaiser Electronics, Litton Applied Technology, and Space Systems / Loral; commercially-oriented firms TRW Semiconductor, Siliconix, and BroadLogic Network Technologies have also enjoyed his services. Bryan has co-authored early studies on electromigration (IRPS 1975), and participated on COMSTAC advisory panels to DOT, on launch-vehicle reliability. Through Ops a La Carte, Bryan has focused on consulting assignments involving circuit analyses for stress/derating, WCA, and FMEA; most projects are military and/or space-bound, with occasional medical equipment tasks. Bryan holds a Physics BS from City University (NY) and an MS in Physics from UCLA, plus an MBA from Santa Clara University. Bryan is a member of APS. With JW Smith, Bryan is exploring ways to propel SPICE and other EDA tools into use downstream and outside of design engineering departments, as an evangelist, consultant, exemplar, and developer.

Mike Silverman is managing partner of Ops A La Carte and has over 25 years experience in reliability engineering, reliability management and reliability training. He is an experienced leader in reliability improvement through analysis and testing. Mike is also an expert in accelerated reliability techniques, including HALT and HASS. He set up and ran an accelerated reliability test lab for 5 years, testing over 300 products for 100 companies in 60 different industries. Through Ops A La Carte, Mike has had extensive experience as a consultant to high-tech companies, and has consulted for over 500 companies including BAE, Lockheed-Martin, Raytheon, Honeywell, Ciena, Siemens, Abbott Labs, and Applied Materials. He has consulted in a variety of different industries including defense electronics, telecommunications, networking, medical, semiconductor equipment, consumer electronics, and power. Mike has authored and published over 15 papers on reliability techniques and has presented these around the world including China, Germany, and Canada. He has also developed and currently teaches over 30 courses on reliability techniques. Mike has a BS degree in Electrical and Computer Engineering from the University of Colorado at Boulder, and is a Certified Reliability Engineer (CRE) through American Society for Quality (ASQ). Mike is a member of ASQ, IEEE, SME, ASME, PATCA, and IEEE Consulting Society. Mike is currently the IEEE Reliability Society Santa Clara Valley Chapter Chair.

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