

# USING EDA THROUGHOUT PRODUCT LIFE-CYCLES

## A More Detailed Look at the Issues

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**The analysis software and design files successfully used in electronic design practice and cycles can also serve well during the rest of the product lifecycle (PLC). The process of PLC-EDA is framed for consideration, and suitable decision criteria are explored. We present a few representative case examples where PLC-EDA is indicated.**

Several classes of challenges routinely arise in ongoing programs in military, aerospace, telecommunication, and medical areas. Unlike in the ephemeral-timescale commercial consumer world, such programs often have significant NRE content, and need long-term life usage to recover the costs invested. Military and medical programs have potentially severe impact on users when they don't quite work as intended, so they also carry significant product qualification investments as part of the NRE. In this setting, PLC use of design files offers an improved way to address issues in parts obsolescence, pattern failure emergences, parts-counterfeiting eruptions, retro-qualification of COTS products, and ex-post-facto agency requirements on subsequent or follow-on orders.

In a previous article entitled "Using EDA Throughout Product Life Cycle", we discussed the overall picture and context into which the insertion of PLC-EDA (use of EDA throughout the product life-cycle) principles makes sense. Here we expand downward from a high level overview to a more detailed look at the issues.

Our intent is multi-purpose:

- i) to help a manager responsible for operating a subsystem-class program decide whether and how PLC-EDA can contribute to the success of the program;
- ii) to inform staff technical contributors supporting agency procurement efforts on how these principles may support or improve the product they are charged with reordering or resolving issues emerging within the indented lower-level components or inputs that make up the products under their cognizance; and
- iii) to provide an outline for technical contributors in involved organizations on how they may orient and prepare themselves and their firms to respond and execute to meet such expectations.

How one goes about deciding and acting is our topic for exploration. The three items above are really one subject, viewed from three perspectives. The world of "serious" systems (i.e. non-consumer, fashion-agnostic, etc) is vastly richer, more complex and convoluted, and more interesting and enduringly rewarding to its participants. It has a fairly simple distinguishing hallmark: unmet expectations are not trivially dealt with by a refund policy and a 90-day guarantee. Problems must be dealt with, responsibly and crisply.

Ideally, a program manager or procurement officer would find her/his internal organizations and vendors already set up for PLC-EDA, practiced into challenge-scenarios, and operationally ready for whatever surprises chance can throw at them. The gap between these naïve expectations and actual reality is not actually that wide. Since virtually all EE graduates in the last 20 years, and many earlier alumni, have had a decent exposure to EDA in academic settings, bridging the gap is mostly a matter of providing all technical staff the pleasing realization that yet another piece of partially forgotten school learning actually has ongoing value.

Surprise problems apparently come at us out of the blue. Or sometimes from a corner of nagging misgivings that we honestly didn't have time to fully resolve because of schedule demands, "borrowed" budgets or staff to address prior eruptions, specification "evolutions", or more. These have the nice feature that we have at least partial foreknowledge, although we may not spend too much time or have the resources to plan full resolution. In spacecraft operations, fully rehearsed "contingency operational procedures" (COPs) are specified and paid for as part of the development NRE. Effective insertion of PLC-EDA is best thought of as similar in spirit. COPs are driven by a "never-again" intolerance of repetitions of very expensive incidents. Within every organization this writer has encountered, there are numerous "war stories" that both identify the local areas of vulnerability to incidents, and define the cultural values of the organization in terms of how they react. PLC-EDA is another weapon to have in the quiver for the next war story.

## CASE STUDIES

Appraising whether/how to insert PLC-EDA is perhaps best contemplated by recalling how it would have contributed to prior product development. Here are a few case studies:

I) A medical device firm received a reorder for an old design, and engaged us to update the FMEA to the 1998 FDA criteria. All documents were bit-mapped images of old drawings, the parts lists had seen several revisions, and none of the design team from 1992 were anywhere in sight. After doing a set of routine circuit FMEAs over the five boards involved, additional requirements dribbled down, from higher-level analyses, requiring essentially three iterations of spreadsheet-level FMEAs generated from the original FMEAs. By this point it became clear that it would have been more cost-effective, and far more detail-rich, especially in the precision of the "mitigation factors" elements, to have constructed EDA models of the five circuits in SPICE from scratch, off the drawings, and use that model for all the analyses. While we were used to using SPICE and other emulators on interesting sub-element areas of complex circuits during WCAs, it was the annoyance of re-doing essentially the same analysis three times that "inspired" the idea that there is an entire class of circuits in existence along the stages of their product lifecycles that are subject to occasionally needed periods of detailed technical reassessment, which informs the foundational idea of PLC-EDA.

II) At a little-remembered startup, consumer receiver boards incorporating a standard switching regulator design were used in a computer system design sold by a next-tier vendor to schools on another continent. One day, a schoolroom incident featuring smoke occurred; the school system suspended use of the computers, and the receiver board, accompanied by a team from the next-

tier firm, arrived at the startup. The failure was quickly identified as a shorted CSR capacitor. Nobody at the startup seemed familiar with the circuit, although a representative from the switching regulator chip house was quite articulate. My offline queries revealed that he in fact made the reference design for that circuit section. In the lab, we ran an actual circuit and witnessed a few hundred transient swings. Actually running a SPICE model confirmed this point. Getting back to the chip vendor's rep, he concurred, helpfully adding that this was precisely why the reference design featured a "low-ESR" version of the capacitor. Armed with this emphasis, we reviewed the parts list and found that, after manufacturing release, a "medium-ESR" version of the cap had been substituted because of availability problems with the low-ESR version, but the cheaper price of the medium-ESR parts had been seen as an extra benefit. Since engineering changes such as this need an engineering sign-off, we asked the signatory what he had been thinking, and, as a good manufacturing engineer, he had checked the substitute drawing for form, fit, and function. There was no design engineering input. There's a moral here: don't just look at the specs; check how the circuit models look under a part substitution. Getting the vendor's already-supplied SPICE model and changing the ESR parameter would require little change beyond the cultural will to do such things. The public relations fallout with the customer on this issue was devastating, and possibly contributed to the startup's venture capitalist's decision to cut funding soon thereafter.

III) During a subsystem Reliability Demonstration Test (RDT) on an avionics electronics box, I had a test-box 5A fuse blown, which traced back to a short on an EMI filter on the 28VDC input supply line. Review of all affected traces showed no vulnerability, and, after appropriate corrective-action efforts, the incident was classified as a "random failure", some additional part screening was imposed, and the test was restarted and ultimately passed. About 18 months later, we received two separate reports of "field incidents" in which pilots reported "smoke in the cabin"; both traced back to the same box, and the same EMI filter. This turned out quite differently from my RDT incident, because the aircraft harness lacked a 5A fuse, but instead featured a breaker set for perhaps 30A or more. When the returned boxes had their EMI filters replaced, that didn't restore functionality because the trace resistance in the affected motherboard limited current under the breaker's setpoint, but well above that needed to damage the motherboard, exceed all the ratings of the epoxy, and "behave" in an unexpected way that even a full suite of flightworthiness tests might not expose. I believe a custom fuse in the harness was retrofitted as a pragmatic response to the situation, but it was done outside of my organizational field-of-view. To this day, I'm not sure whether a spec imposing robustness to 30A during a short circuit condition would represent improvement, but at the system level of our customer, the ability to take note of a 5A fuse blow in the application context of no-fuse use, and recognize its potential impact, could have allowed much earlier and better resolution of the issue. PLC-EDA usage may be an effective tool in modeling such incidents at the higher level.

Case studies define the envelope of topics where PLC-EDA can contribute to an enterprise's efforts. Repetitive incident types or similar resolutions are a strong sign that opportunity for improvement exists in a definite area. Then inaction becomes indefensible.

## CASES THAT ARISE WHERE PLC-EDA MAY HELP

Abstracting common features from the war stories, and applying creative common-sense extensions to normal activities, we can form a list of EDA-accessible circuit/system dynamics to consider:

- 1) Changes in transient response, circuit stability, or EMI issues
- 2) Compromises in performance windows, derating or EOL margins
- 3) Possible changes in FMEA propagation
- 4) Emulation of redundancy-switching schemes, majority-voting circuitry
- 5) Validation of BIT-coverage expectations, and identification of "holes"
- 6) Scenario-modeling of latent degradation from prior-incident overstress
- 7) Review of repetitive field failures or failure-pattern combination occurrences

Items 1-4 are the categorical areas that PLC-EDA analysis can enhance. These areas are generally covered extensively during design cycles, and at some point, spec compliance is achieved. The compliance package generically scopes the set of analyses deemed worthy of consideration. In subsequent PLC-EDA work, this set is a minimum, not a maximum, because in field contexts problems emerge independent of analyses, and it is plain good luck if such problems fit neatly under one specific analysis heading.

Items 5-7 are more extensive add-on uses that "go beyond" the minimum set, but without PLC-EDA they are usually waived as open-ended exercises. They both need deep familiarity with circuit functionality, but they are contrary to a design engineer's normal ethos, and so the synthetic familiarity that PLC-EDA gives to a second-set-of-eyes enables dispassionate third-party reviews to a satisfactory level.

There is an art to picking worthwhile activities, instead of mindlessly imposing every conceivable requirement and squandering resources without meaningful return. This applies to PLC-EDA too.

## STRAIGHTFORWARD RECIPE IN PLC-EDA PRACTICE

While surprise situations all have their unique traits, a minimal recommended flow for addressing "incidents", or scoping out a program, is:

- A) Identify new questions, proposed change(s), or issues
- B) Determine scope of reviews and analyses to be revised
- C) Generate or acquire/resurrect suitable EDA model
- D) Characterize before/after by several simulation runs to elucidate significant features, or bring them out if the documentation package is "inadequate"
- E) Act on data, iterate as indicated

Life can be easier if you can stage a rehearsal to wring out your in-house "local color" attributes. It is easier to pretend an issue has arisen and then quickly plan a response using available resources. Either in rehearsal or in real-incident cases, there is a learning-curve process that occurs, and the experience value does accumulate.

## KEY TAKEAWAY

The same analysis software so successfully established in electronic design practice can also serve well during the rest of the product lifecycle. No real barriers exist except the decision to begin. And for helping you with this process, please call on the reliability consultants at Ops A La Carte to help.

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## BIOGRAPHIES

**Bryan Stallard** is a senior reliability consultant at Ops A La Carte with over 30 years experience in analysis, design, and testing of electronic products, spanning the scale from junction diodes to satellite bus systems. He has worked on aviation electronics displays (A-6, A-10, F16, F18, Cobra), radar-warning receivers (ALR-45, ALR-67, ALR74), and satellite families (INTELSAT, GOES, SUPERBIRD, Space Station) as circuit analyst, program reliability engineer, RF designer, component engineer, failure-lab analyst, and combination-activity roles. He is culturally familiar with military, NASA, commercial aerospace, semiconductor, and telecom practices and expectations. Employers included Kaiser Electronics, Litton Applied Technology, and Space Systems / Loral; commercially-oriented firms TRW Semiconductor, Siliconix, and BroadLogic Network Technologies have also enjoyed his services. Bryan has co-authored early studies on electromigration (IRPS 1975), and participated on COMSTAC advisory panels to DOT, on launch-vehicle reliability. Through Ops a La Carte, Bryan has focused on consulting assignments involving circuit analyses for stress/derating, WCA, and FMEA; most projects are military and/or space-bound, with occasional medical equipment tasks. Bryan holds a Physics BS from City University (NY) and an MS in Physics from UCLA, plus an MBA from Santa Clara University. Bryan is a member of APS. With JW Smith, Bryan is exploring ways to propel SPICE and other EDA tools into use downstream and outside of design engineering departments, as an evangelist, consultant, exemplar, and developer.

**Mike Silverman** is managing partner of Ops A La Carte and has over 25 years experience in reliability engineering, reliability management and reliability training. He is an experienced leader in reliability improvement through analysis and testing. Mike is also an expert in accelerated reliability techniques, including HALT and HASS. He set up and ran an accelerated reliability test lab for 5 years, testing over 300 products for 100 companies in 60 different industries. Through Ops A La Carte, Mike has had extensive experience as a consultant to high-tech companies, and has consulted for over 500 companies including BAE, Lockheed-Martin, Raytheon, Honeywell, Ciena, Siemens, Abbott Labs, and Applied Materials. He has consulted in a variety of different industries including defense electronics, telecommunications, networking, medical, semiconductor equipment, consumer electronics, and power. Mike has authored and published over 15 papers on reliability techniques and has presented these around the world including China, Germany, and Canada. He has also developed and currently teaches over 30 courses on reliability techniques. Mike has a BS degree in Electrical and Computer Engineering from the University of Colorado at Boulder, and is a Certified Reliability Engineer

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